WHAT IS CLAIMED IS:

1. A computer based test bench generator for verifying integrated circuits specified by models in a Hardware Description Language, comprising:

a repository storing a general set of self-checking tests applicable to integrated circuits;

means for entering behavior data of an integrated circuit model;

means for entering configuration data of the integrated circuit model;

means for automatically generating test benches in said Hardware Description Language, said means being configured to make a selection and setup of suitable tests from said repository according to the specified integrated circuit model, configuration and behavior data.

2. The test bench generator of claim 1, wherein said integrated circuit model is a memory model.

3. The test bench generator of claim 1, wherein said general set of tests is specified in said Hardware Description Language.

4. The test bench generator of claim 2, wherein said Hardware Description Language is VERILOG.

5. The test bench generator of claim 3, wherein said behavior data is specified in a proprietary language.

6. The test bench generator of claim 3, wherein said configuration data is inputt to said generator through a command line.

7. The test bench generator of claim 3, wherein said selection of tests is based on conditional statements.

8. A method for verifying integrated circuits specified by integrated circuit models in a Hardware Description Language, comprising the steps of:

storing a general set of self-checking tests applicable to integrated circuits in a repository;

entering behavior data of an integrated circuit model;

entering configuration data of the integrated circuit model;

selecting and setting up suitable tests from said repository according to the specified integrated circuit model, configuration and behavior data, so as to generate test benches in said Hardware Description Language.

9. The method according to claim 8, wherein said integrated circuit model is a memory model.

10. The method according to claim 8, wherein said general set of tests is specified in said Hardware Description Language.

11. The method according to claim 10, wherein said Hardware Description Language is VERILOG.

12. The method according to claim 11, wherein said behavior data is specified in a proprietary language.

13. The method according to claim 11, wherein said configuration data is input to said generator through a command line.

14. The method according to claim 11, wherein said selection of tests is based on conditional statements.

15. A test bench generator for integrated circuit designs, comprising:

a repository which stores functional and structural characteristic data for integrated circuit models;

a processing functionality which receives an identification of a specific integrated circuit model to be tested along with model data describing the configuration and behavior of that specific integrated circuit model, the processing functionality operating to:

process the model data in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation; and

compare the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model.

16. The generator of claim 15 wherein the processing functionality further processes the identified tests which are applicable to produce a set of self-checking test benches for the specific integrated circuit model.

17. The generator of claim 16 wherein the self-checking test benches are Verilog test benches.

18. The generator of claim 16 wherein the self-checking test benches include self-checking models incorporating complex constructs for comparing data, waiting for internal events, and timing constraint checking with respect to the specific integrated circuit model.

19. The generator of claim 15 wherein the integrated circuit models in the repository, as well as the received specific integrated circuit model to be tested, are specified using a hardware description language.

20. The generator of claim 19 wherein the hardware description language is a Verilog language.

21. The generator of claim 15 further including a simulator functionality which applies the identified applicable tests against the configured integrated circuit model.

22. A test bench generation method for integrated circuit designs, comprising:

storing functional and structural characteristic data for integrated circuit models;

receiving an identification of a specific integrated circuit model to be tested along with model data describing the configuration and behavior of that specific integrated circuit model;

processing the model data in view of the identified specific integrated circuit model to produce a configured integrated circuit model suitable for simulation; and

comparing the specific integrated circuit model to characteristic data in the repository to identify tests applicable to that specific integrated circuit model.

23. The method of claim 22 further including processing the identified tests which are applicable to produce a set of self-checking test benches for the specific integrated circuit model.

24. The method of claim 23 wherein the self-checking test benches are Verilog test benches.

25. The method of claim 23 wherein the self-checking test benches include self-checking models incorporating complex constructs for comparing data, waiting for internal events, and timing constraint checking with respect to the specific integrated circuit model.

26. The method of claim 22 wherein the integrated circuit models in the repository, as well as the received specific integrated circuit model to be tested, are specified using a hardware description language.

27. The method of claim 26 wherein the hardware description language is a Verilog language.

28. The method of claim 22 further including applying the identified applicable tests against the configured integrated circuit model to simulate operation.